IDEC Chip Design Contest

Time domain radar SoC for object recognition using sliding-scan and ultra-fast sampling techniques

Sang Ho Rhee, Hyun Min Kim, Tae Wook Kim

Department of Electrical and Electronic Engineering, College of Engineering, Yonsei University, Republic of Korea

Abstract

Keywords – Sliding-scan, Time-Domain radar

This paper presents a novel radar system that identifies targets based on their inherent characteristics, aiming to overcome the limitations of conventional designs and improve overall system performance. By operating in the time domain and learning impulse signals, the proposed system enables the recognition of stationary objects. Reflected waveforms inherently contain target-specific features, which are exploited by AI-based waveform learning for object classification. To address the structural limitations and instability of traditional timing-path-based architectures, such as sensitivity to noise, high complexity, and risk of oscillation, the proposed system adopts a sliding-scan technique. This method incrementally shifts the sampling window in each cycle to scan the detection range, thereby enhancing receiver sensitivity and extending detection coverage. The simplified architecture reduces both area and power consumption. In addition, the elimination of feedback loops improves circuit stability. Once the target position is detected, high-speed sampling is performed at that location to reconstruct the waveform, implemented using a digital FPGA platform. The proposed system shows promise for applications beyond gesture recognition, including automotive radar.

Introduction

A. System Description

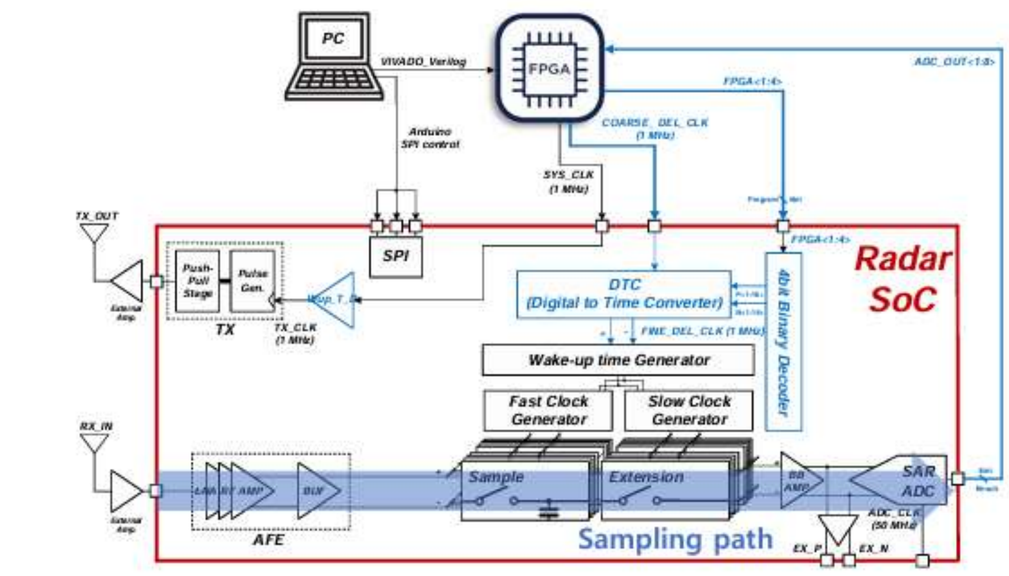

Fig 1. Block Diagram of the Proposed System

The proposed Radar SoC eliminates traditional timing path components such as the envelope detector and TDC, simplifying the architecture. Instead, it adopts a Sliding-scan technique using only the sampling path to detect the precise timing of received signals.

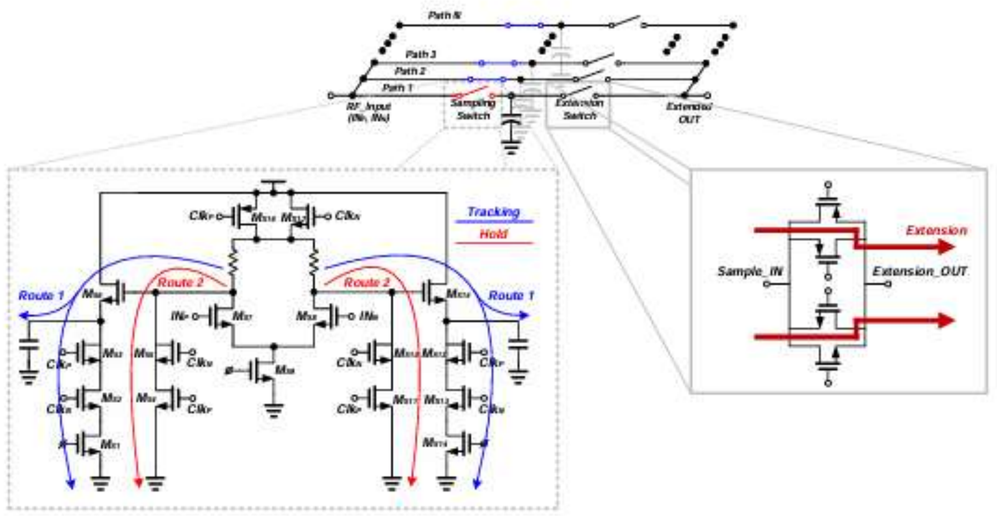

Fig 2. Sample & Extension Block: Schematic and Operation

The core of the sliding-scan sampling path is the Sample & Extension block. The system uses 40 of these blocks to sample high-speed input signals and temporarily store them in holding capacitors. Operating at up to 33 GS/s, each block samples the signal and holds it. The Extension switch converts the high-speed sampled data into a continuous 50 MHz signal during the dead time.

Acknowledgement The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

Each Sample & Extension block operates in a Track & Hold manner. When the source follower is on, Route 1 is activated to track the input. Once the fast clock turns off the source follower, Route 2 activates and transfers the signal to the holding capacitor. After sampling via Path 1, Path 2 begins sampling, enabling seamless sampling across all 40 blocks in sequence.

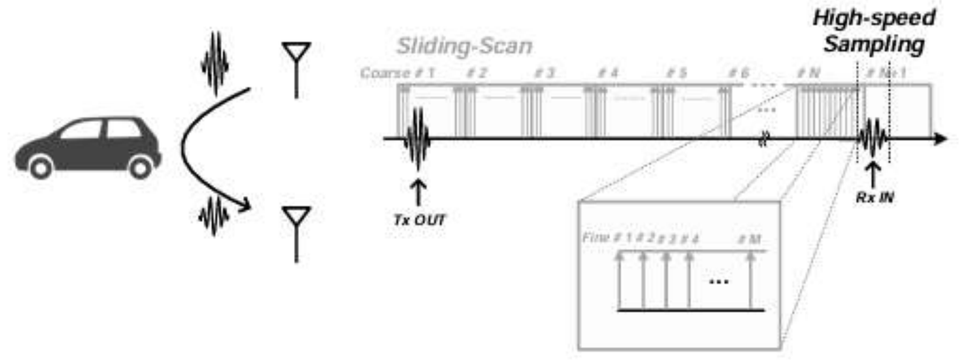

Fig 3. Sliding-Scan and High-Speed Sampling

The proposed sliding-scan method detects the arrival time of received signals by shifting the sampling window in two steps: Coarse and Fine. This replaces the conventional timing-path approach. By scanning the detection range, the system identifies the approximate signal location and converts it to digital data via an ADC, which is then sent to an FPGA. The FPGA stores the data and, upon determining the arrival window, performs high-speed sampling at that location to reconstruct the waveform with high precision.

B. System Implementation

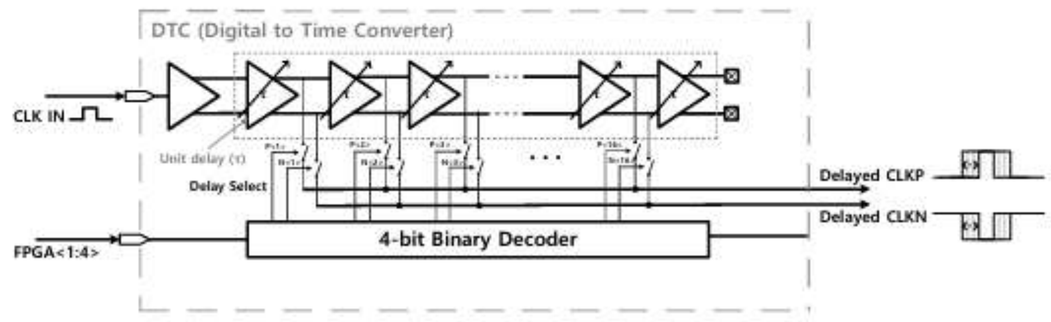

Fig 4. 4-bit DTC + Binary Decoder Block Diagram

The DTC block generates fine delay steps for sliding-scan sampling using 16-unit delay cells. A 4-bit code from the FPGA selects one delay path through a binary decoder, enabling only the corresponding output. The unit delay is tunable from 1 ns to 1.5 ns via SPI, allowing precise alignment with sampling periods from 1 ns (40 GHz) to 2 ns (20 GHz).

Results

	This work	[1], [2]	[3]	[4]
Frequency	3 - 5 GHz	57 ~ 64 GHz	145 GHz	4GHz
Channel	1TX + 1RX	2TX + 4RX	1TX + 1RX	1TX + 1RX
Feature	Pulse radar	FMCW radar	FMCW radar	Pulse radar
Sampling Speed	20 ~ 33 GS/s	N/A	N/A	N/A
Power Consumption	58.3 mW	990 mW	500 mW	260 mW
Rx sensitivity	-65 dBm	N/A	N/A	-45 dBm
Chip Size	3.6 mm^2	20.25 mm^2	6.5 mm^2	2.1 mm^2
Process	65 nm CMOS	0.35 um SiGe	28 nm CMOS	0.13 um CMOS

Table 1. Performance Comparison

As shown in Table 1, our radar system offers low power consumption, small chip area, and high sampling speed, while maintaining reliable sensitivity. This demonstrates its suitability for compact and efficient radar applications.

[1] J. Lien, "Soli: Ubiquitous gesture sensing with millimeter wave radar," ACM Trans. Graph., vol. 35, p. 142, Jul. 2016.

[2] I. Nasr et al., "A highly integrated 60 GHz 6-channel transceiver with antenna in package for smart sensing and short-range communications," IEEE J. Solid-State Circuits, vol. 51, no. 9, pp. 2066–2076, Sep. 2016.

[3] A. Visweswaran et al., "9.4 A 145GHz FMCW-Radar Transceiver in 28nm CMOS," 2019 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 168-170

[4] Y. Shim et al., "A 520 pJ/pulse IR-UWB radar for short range object detection," 2011 IEEE Radio Frequency Integrated Circuits Symposium, Baltimore, MD, USA, 2011, pp. 1-4

Conclusion

This work proposes a time-domain radar system for object recognition using sliding-scan and high-speed sampling techniques. By removing the traditional timing path and adopting a sampling-based approach, the system simplifies design and improves stability. A two-step sliding-scan (Coarse + Fine) locates signal timing, implemented with on-chip DTC + binary decoder and external FPGA control. The system achieves low power consumption (58.3 mW) and high sensitivity (−65 dBm), demonstrating potential for vehicle radar applications.